

EE 330

Lecture 10

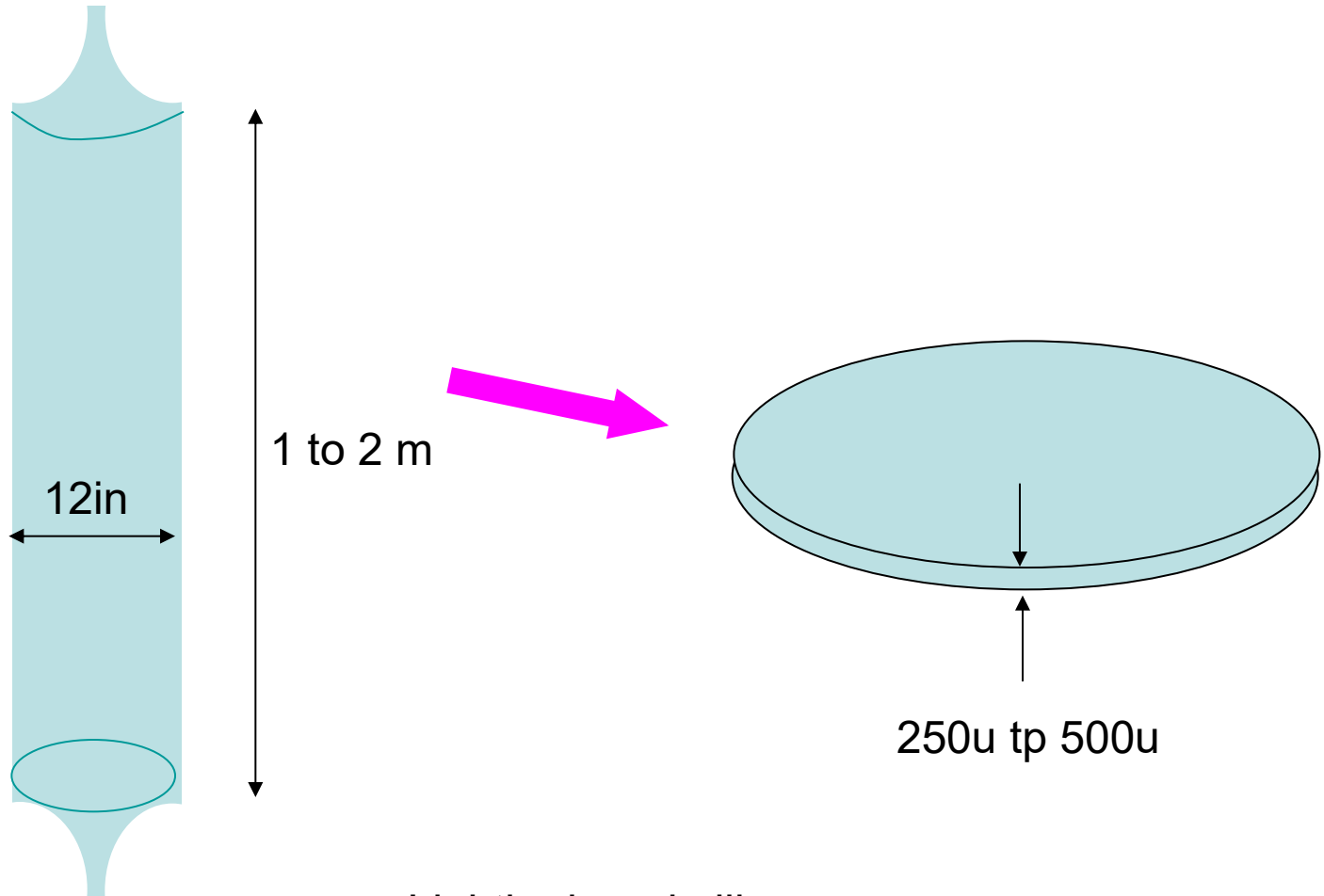
IC Fabrication Technology

- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect, and Metallization

Fall 2024 Exam Schedule

Exam 1 Friday Sept 27

Crystal Preparation



Some predict newer FABs to be at 450mm (18in) by 2020 but appears to be uncertain whether it will ever happen

Lightly-doped silicon
Excellent crystalline structure

Review from Last Time

Masking



Mask Features

Photolithographic Process

- Photoresist
 - Viscous Liquid
 - Uniform Application Critical (spinner)
 - Baked to harden
 - Approx 1 μ thick
 - Non-Selective
 - Types
 - Negative – unexposed material removed when developed
 - Positive-exposed material removed when developed
 - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
 - Exposure
 - Projection through reticle with stepper (scanners becoming popular)
 - Alignment is critical !!
 - E-Beam Exposures
 - Eliminate need for reticle
 - Capacity very small
- Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size

Deposition


- Application of something to the surface of the silicon wafer or substrate
 - Layers 15A to 20u thick
- Methods
 - Physical Vapor Deposition (nonselective)
 - Evaporation/Condensation
 - Sputtering (better host integrity)
 - Chemical Vapor Deposition (nonselective)
 - Reaction of 2 or more gases with solid precipitate
 - Reduction by heating creates solid precipitate (pyrolytic)
 - Screening (selective)
 - For thick films
 - Low Tech, not widely used today

Ion Implantation

Application of impurities into the surface of the silicon wafer or substrate

- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security

IC Fabrication Technology

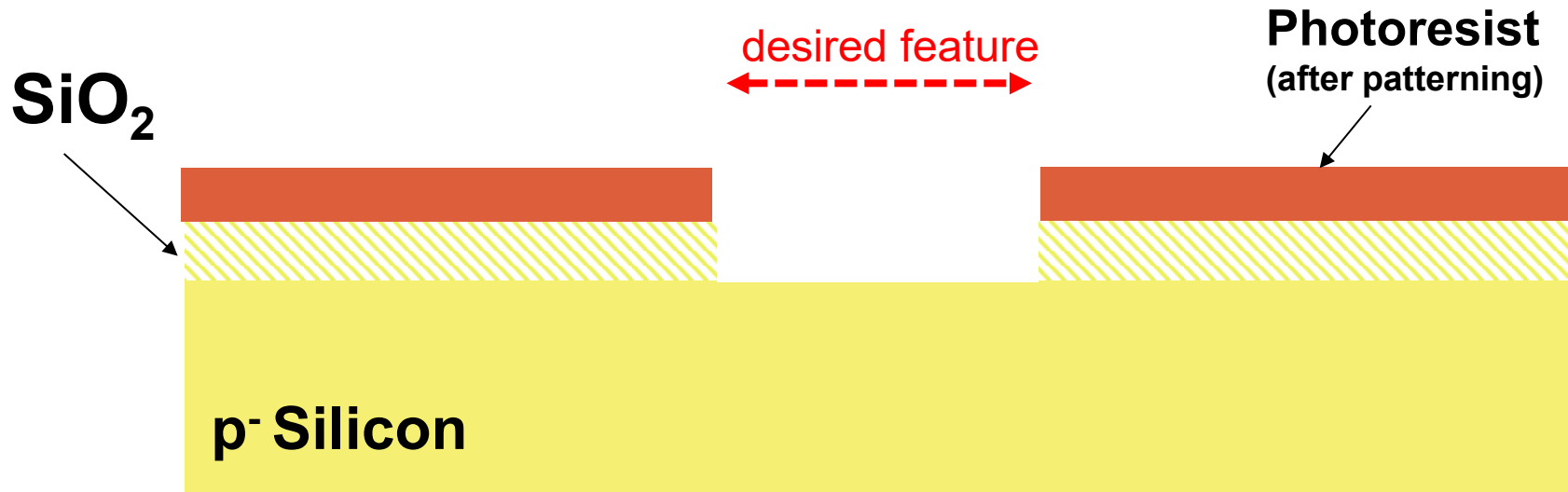
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Etching

Selective Removal of Unwanted Materials

- Wet Etch
 - Inexpensive but under-cutting a problem
- Dry Etch
 - Often termed ion etch or plasma etch

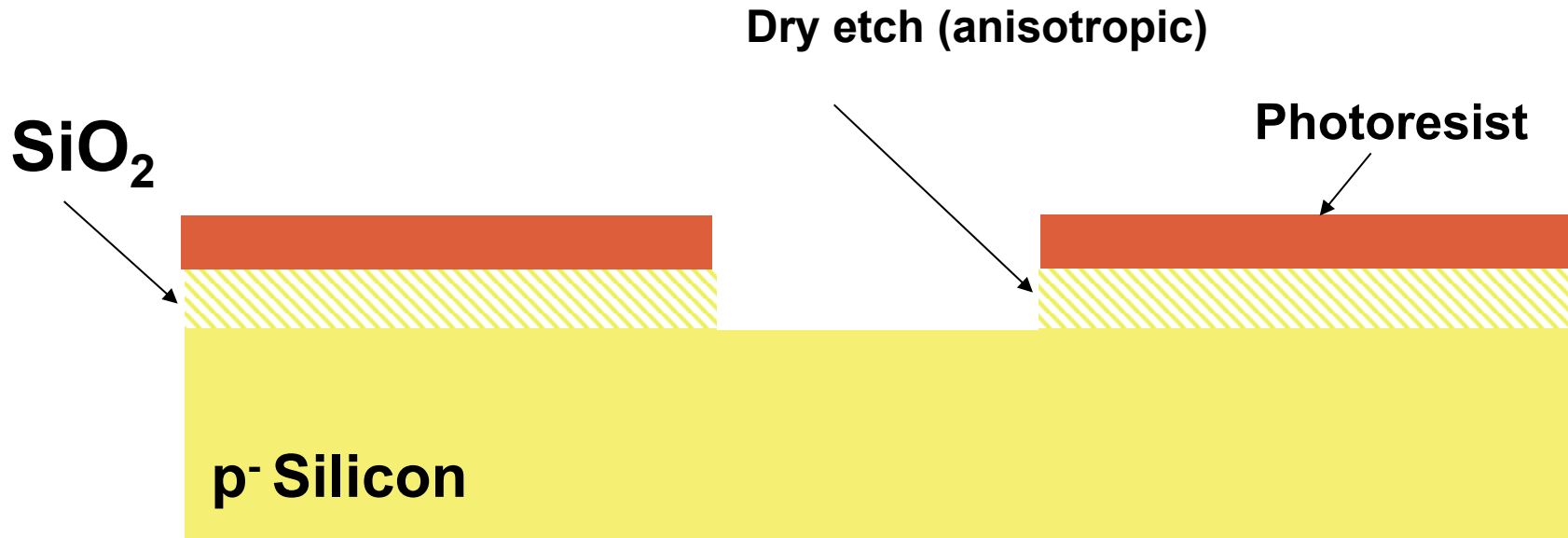
Etching



Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about $\frac{1}{2}$ order of magnitude larger than lateral dimensions

Etching



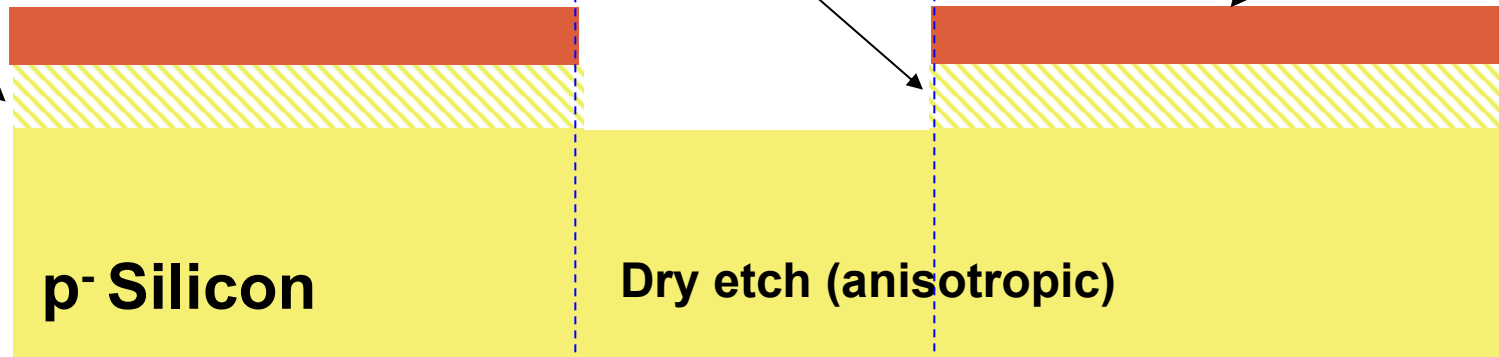
Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist patterning)

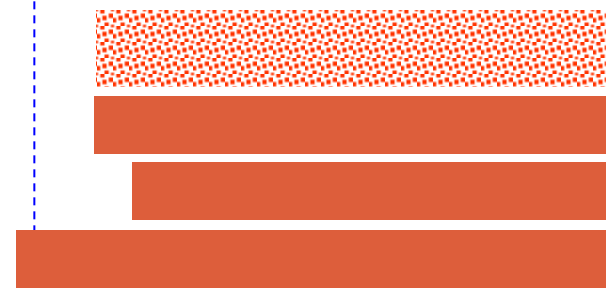
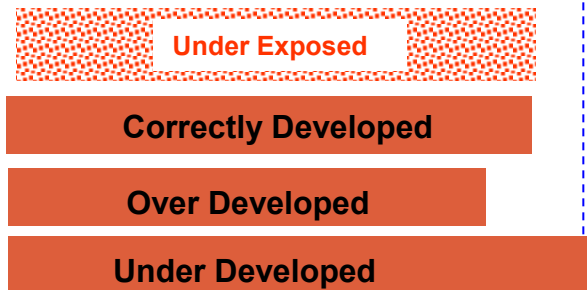
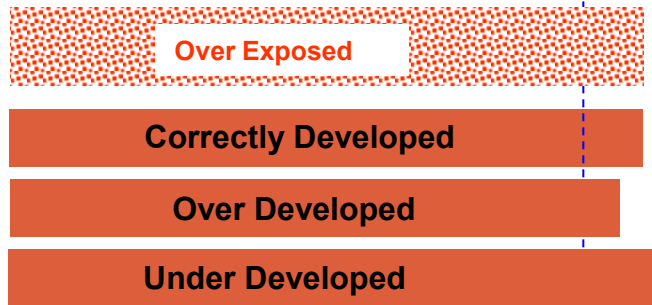
Etching (limited by photolithographic process)

SiO_2

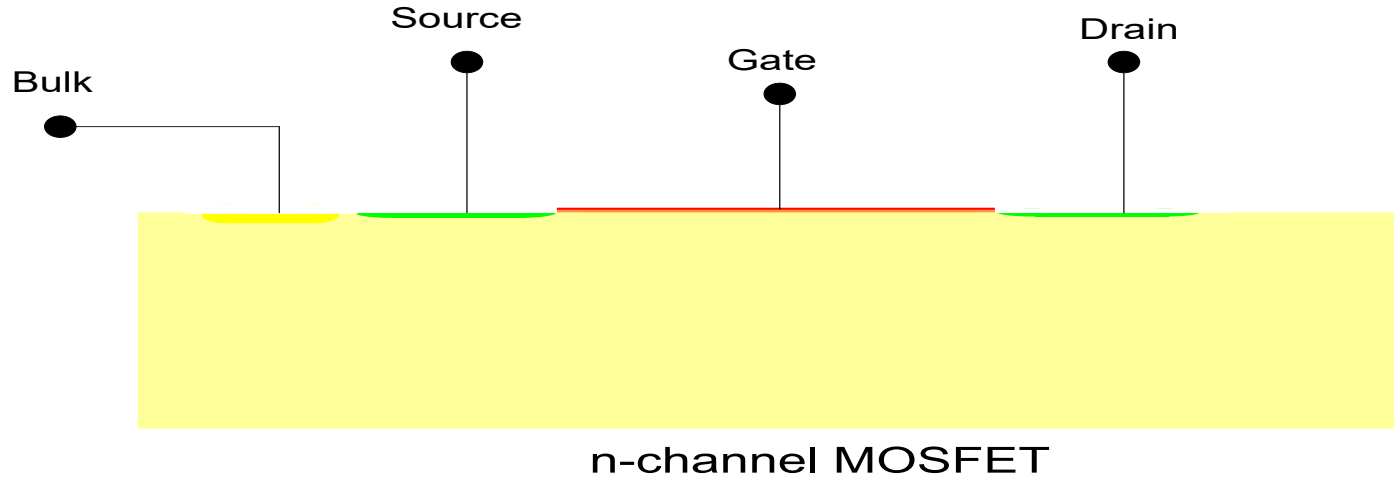
Dry etch (anisotropic) Photoresist



Consider neg photoresist (unexposed removed)



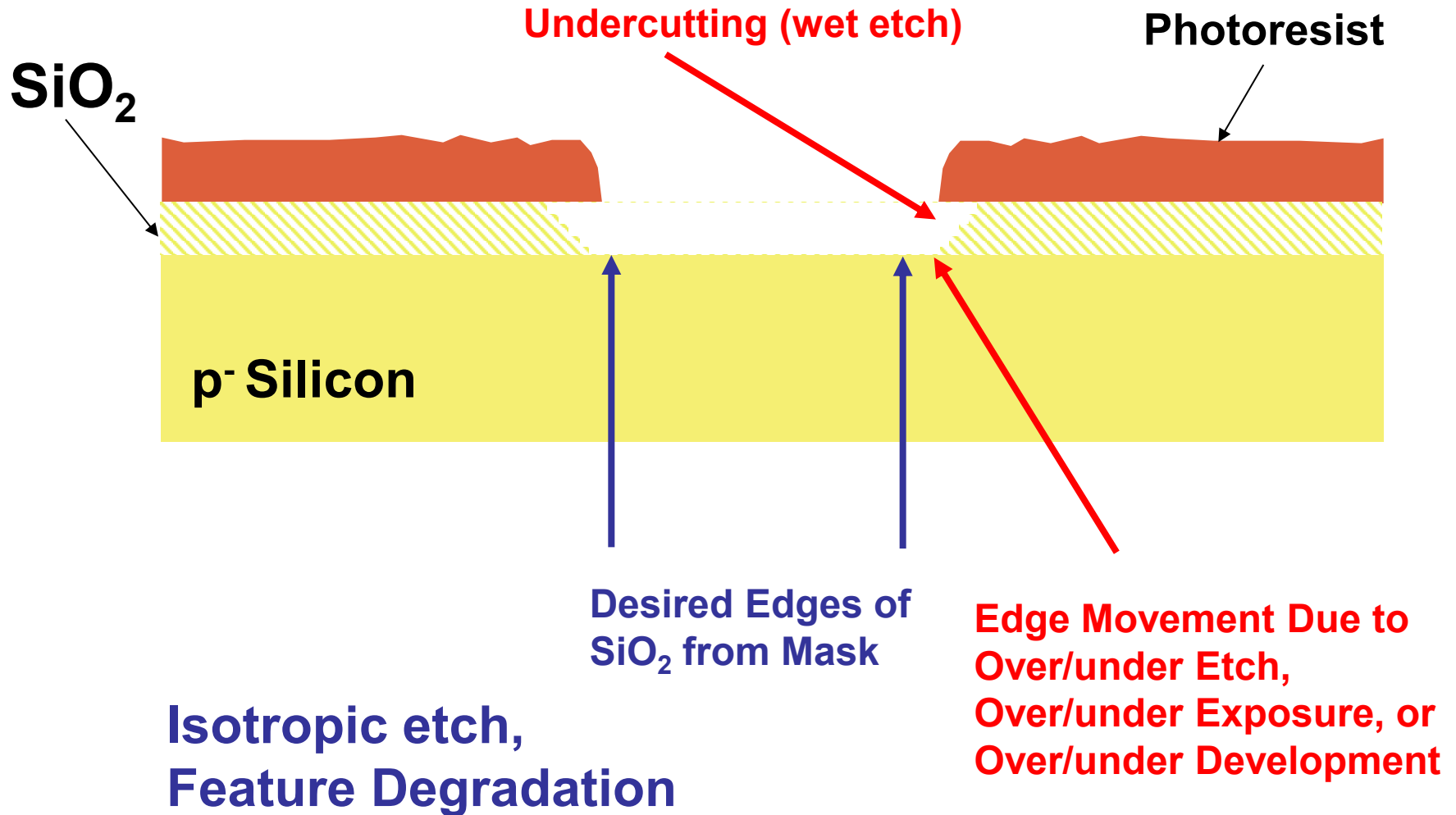
Lateral Relative to Vertical Dimensions



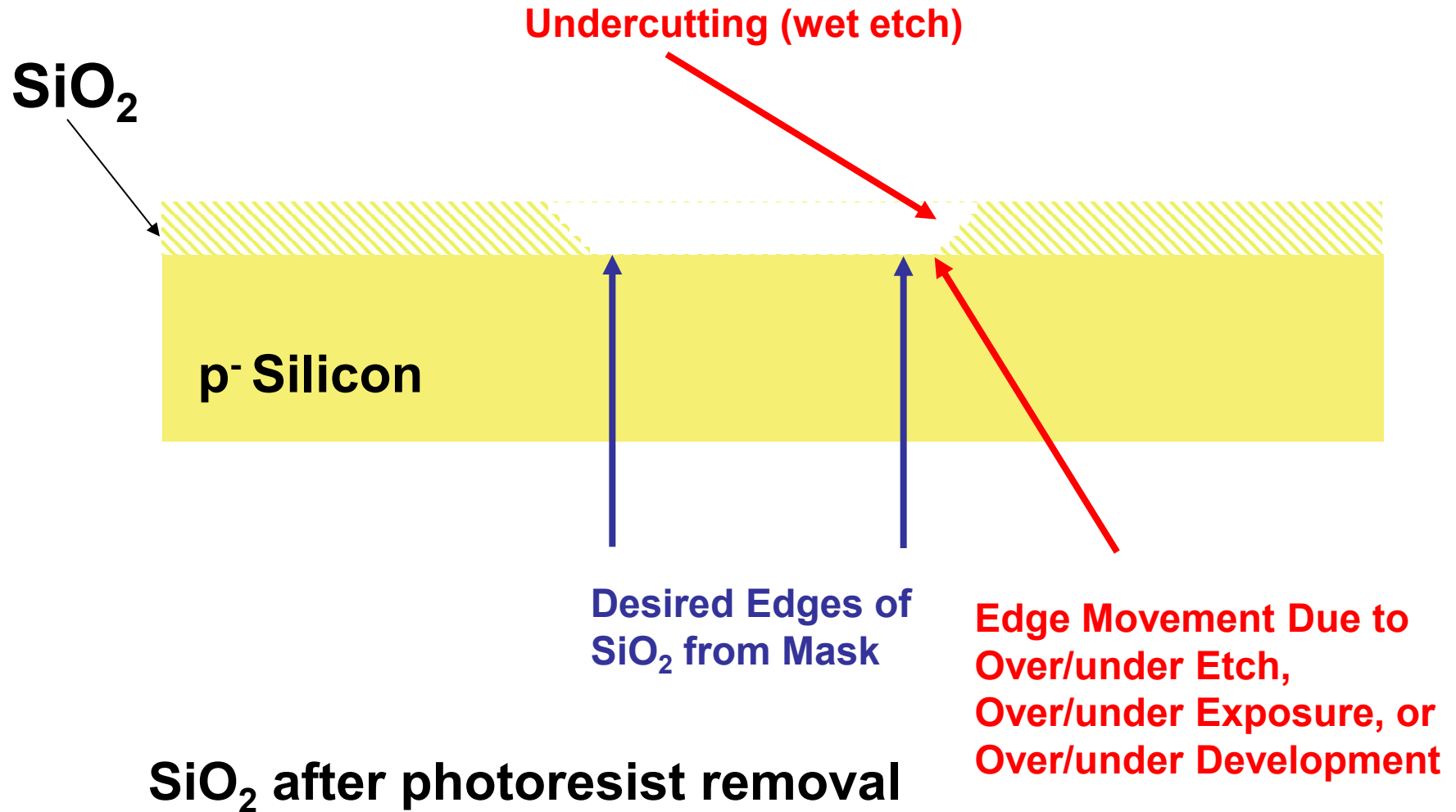
Still Not to Scale

For Example, the wafer thickness is around 250 μ and the gate oxide is around 50 \AA (5E-3 μ) and diffusion depths are around $\lambda/5$

Etching



Etching



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Diffusion

- Controlled Migration of Impurities
 - Time and Temperature Dependent
 - Both vertical and lateral diffusion occurs
 - Crystal orientation affects diffusion rates in lateral and vertical dimensions
 - Materials Dependent
 - Subsequent Movement
 - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
 - Diffusion at 800°C to 1200°C
- Source of Impurities
 - Deposition
 - Ion Implantation
 - Depth depending on ion speed/energy
 - More accurate control of doping levels
 - Fractures silicon crystalline structure during implant
 - Annealing occurs during diffusion
- Types of Impurities
 - n-type Arsenic, Antimony, Phosphorous
 - p-type Gallium, Aluminum, Boron

Diffusion

Source of Impurities Deposited on Silicon Surface



Before Diffusion



After Diffusion

Diffusion

Source of Impurities Implanted in Silicon Surface



p⁻ Silicon

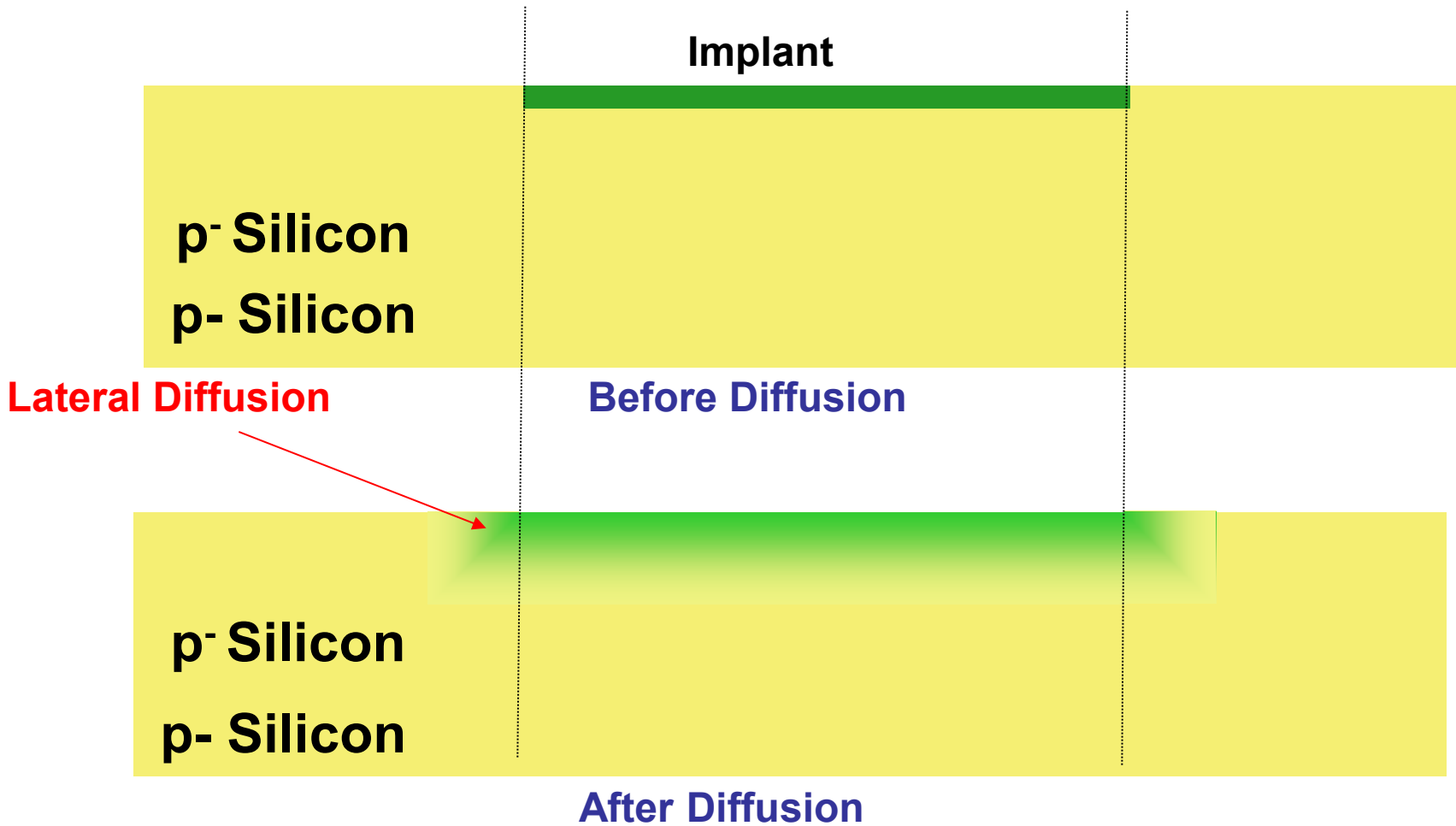
Before Diffusion

p⁻ Silicon

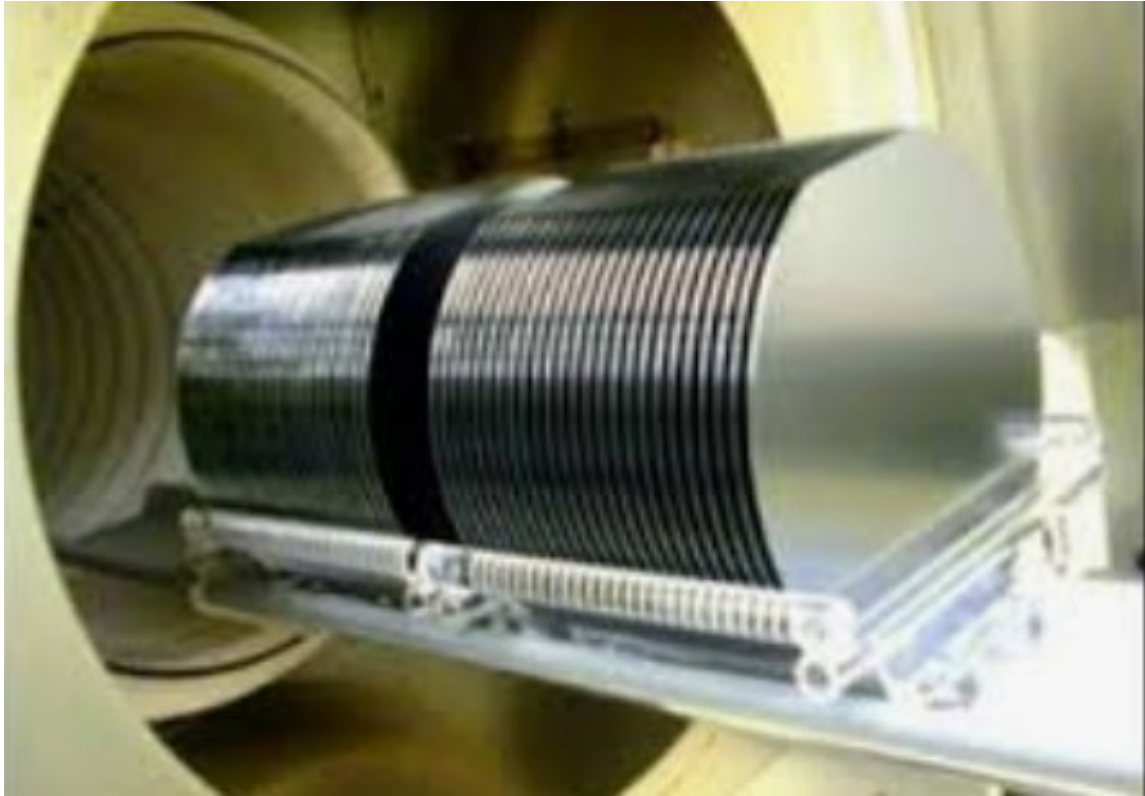
After Diffusion



Diffusion

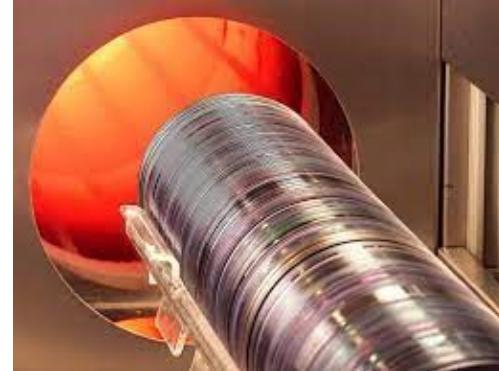


Diffusion



300mm wafers loading in diffusion furnace

Diffusion



Temperature for diffusion of impurities in silicon: 900°C to 1100°C

Time, temperature, uniformity, and time-temperature profile strongly effect properties of semiconductor devices

Melting point of Silicon: 1420°C (Poly around 1414°C)

Melting point of SiO₂: 1710°C

Melting point of Aluminum: 660°C

Melting point of Copper: 1085°C

Melting point of Quartz: 1670°C

Very approximately: diffusion rate targeted at 1um/hour

Very approximately: diffusion depths from 0.5um to 30um

Diffusion rate extremely low (but not 0) at normal operating temperatures

IC Fabrication Technology

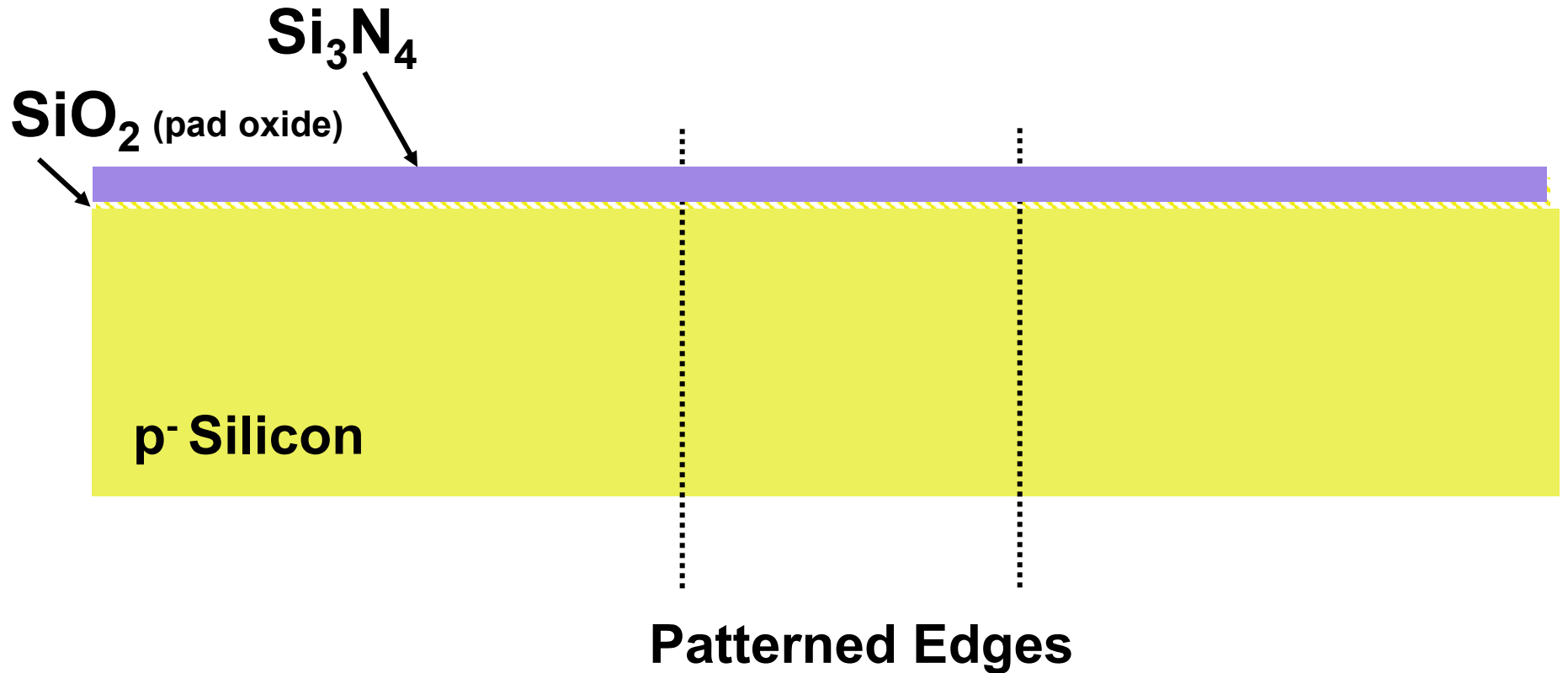
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Oxidation

- SiO_2 is widely used as an insulator
 - Excellent insulator properties
- Used for gate dielectric
 - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
 - termed field oxide
 - field oxide layers very thick
- Methods of Oxidation
 - Thermal Growth (LOCOS)
 - Consumes host silicon
 - x units of SiO_2 consumes .47x units of Si
 - Undercutting of photoresist
 - Compromises planar surface for thick layers
 - Excellent quality
 - Chemical Vapor Deposition
 - Needed to put SiO_2 on materials other than Si

Oxidation

Thin layer of Silicon Nitride is deposited (serves as oxidation barrier)

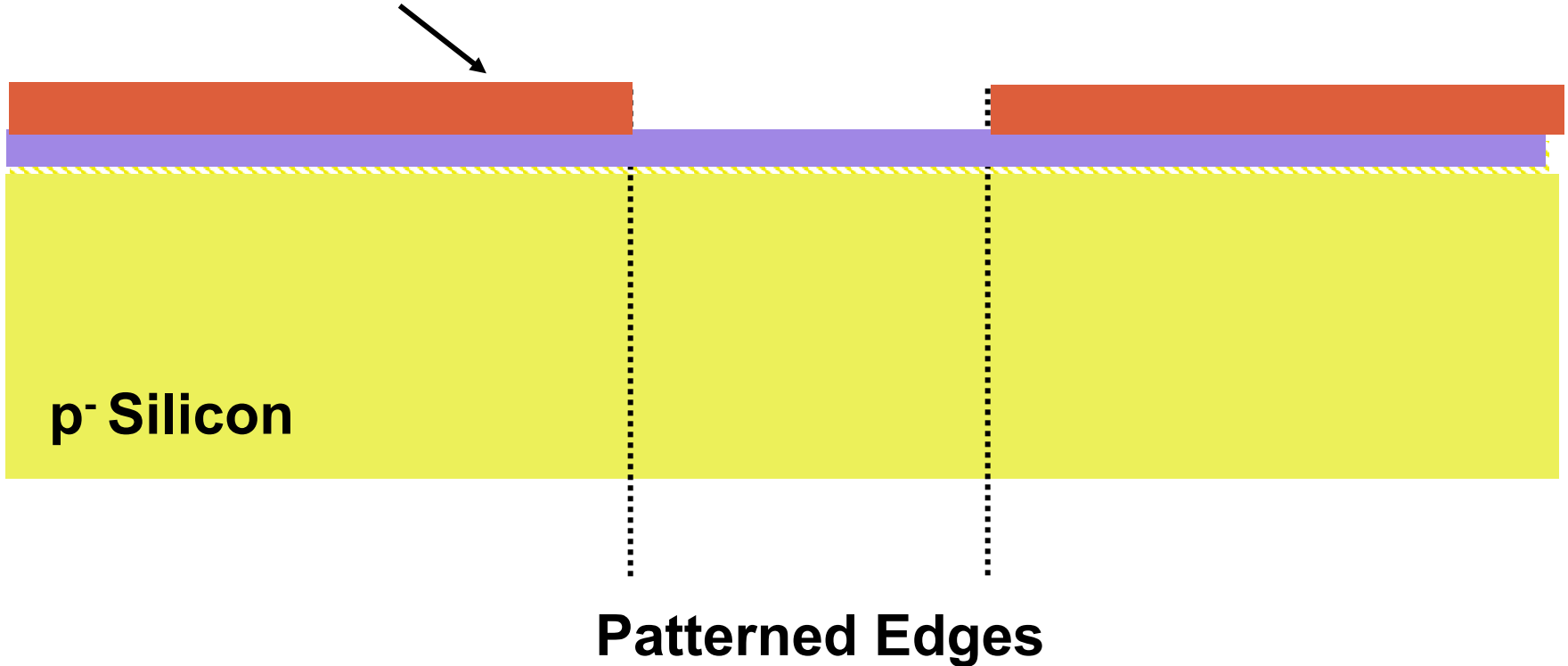


Thermally Grown SiO₂ (LOCOS) - desired growth

Oxidation

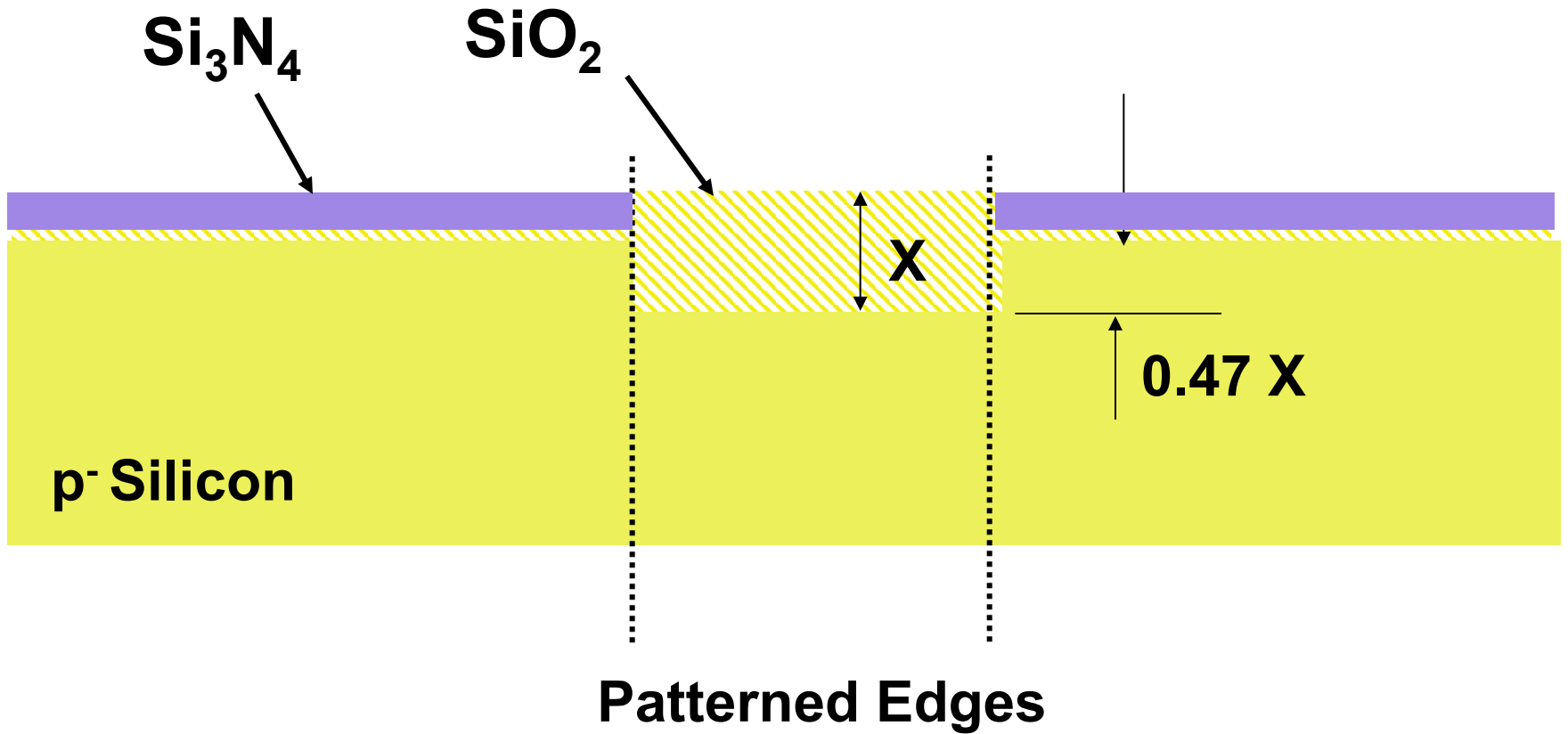
Silicon Nitride Patterned with Photoresist

Photoresist



Thermally Grown SiO_2 - desired growth

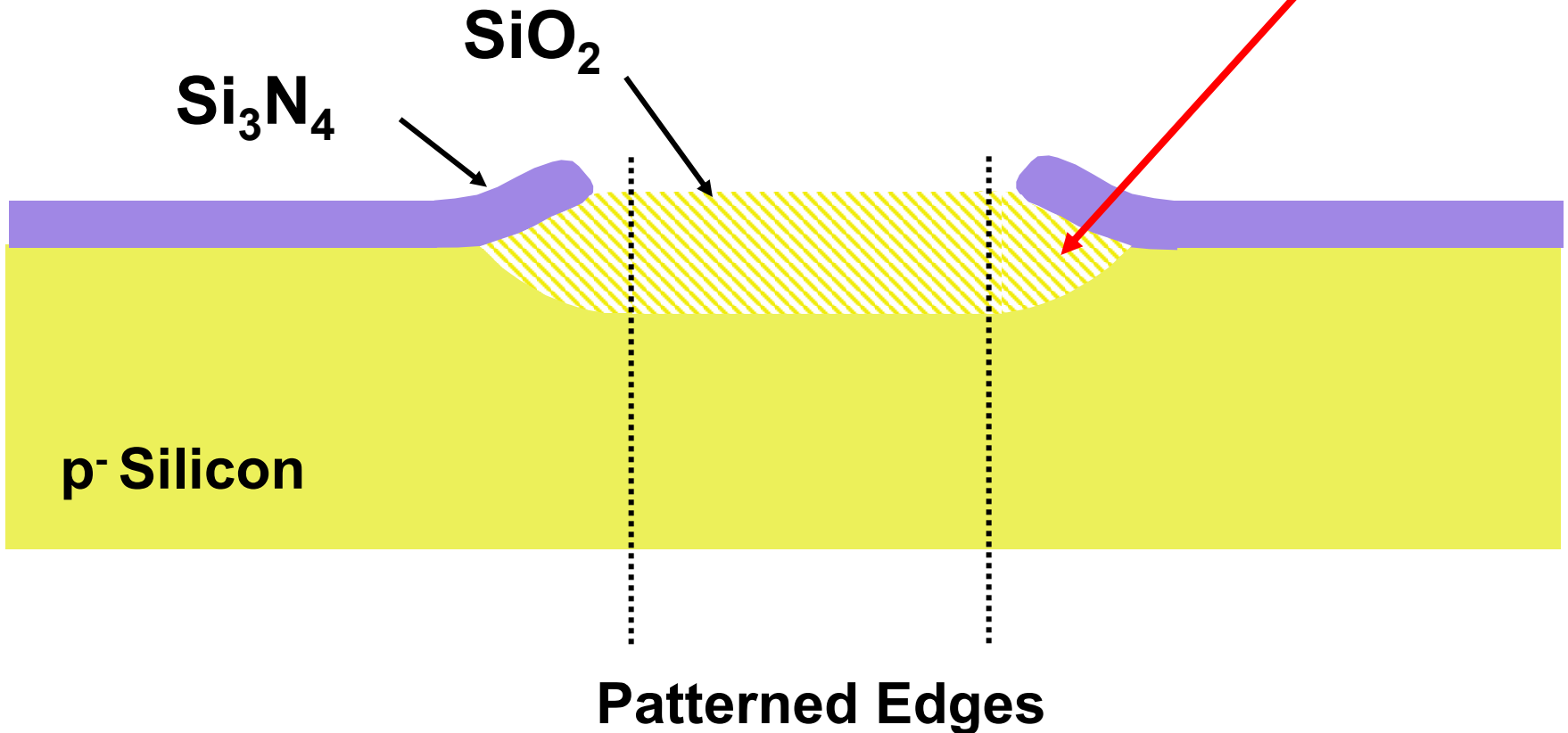
Oxidation



Thermally Grown SiO_2 - desired growth

Oxidation

Bird's Beaking

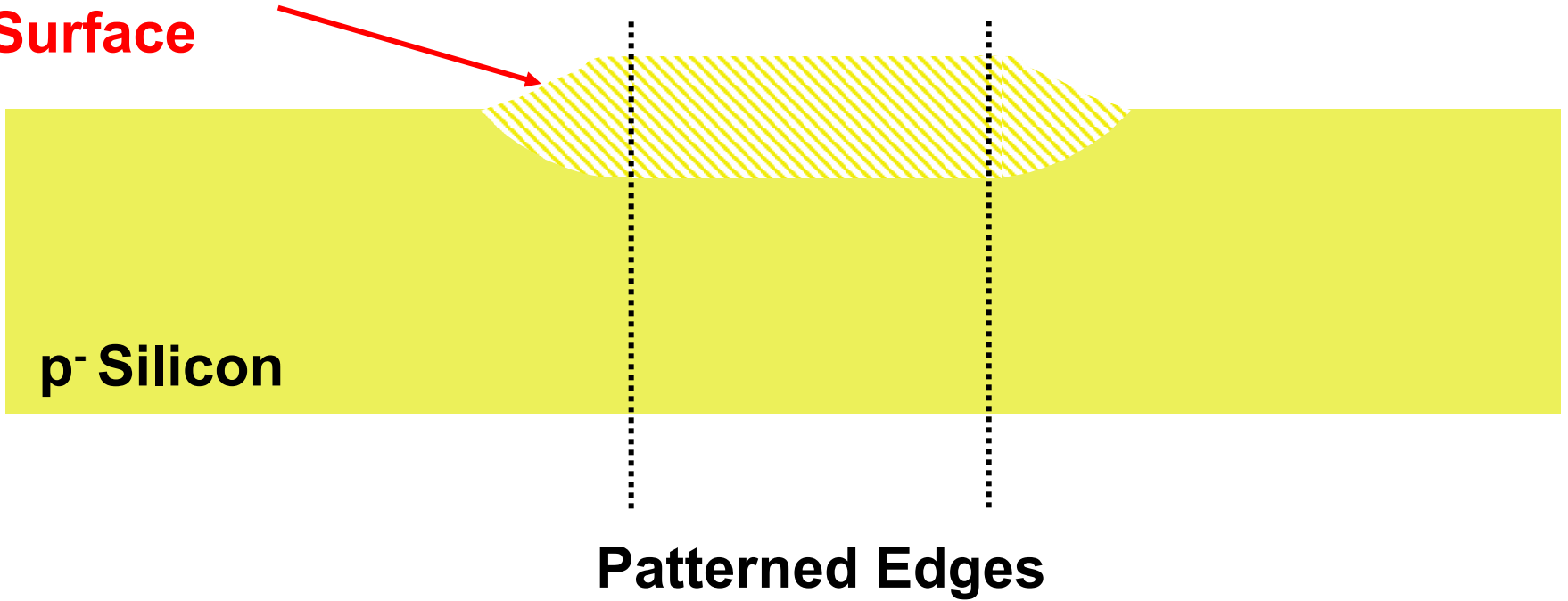


Thermally Grown SiO₂ - actual growth

Oxidation

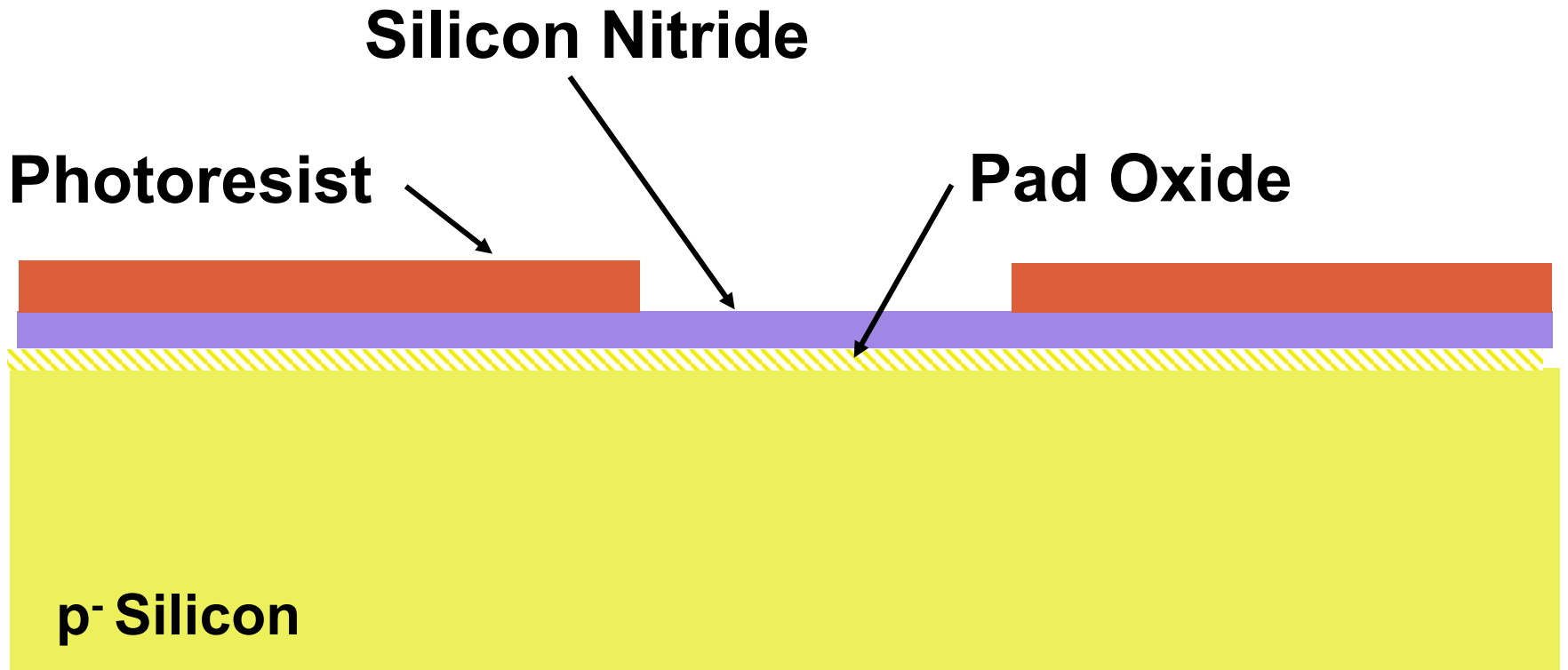
After removal of Si_3N_4

**Nonplanar
Surface**



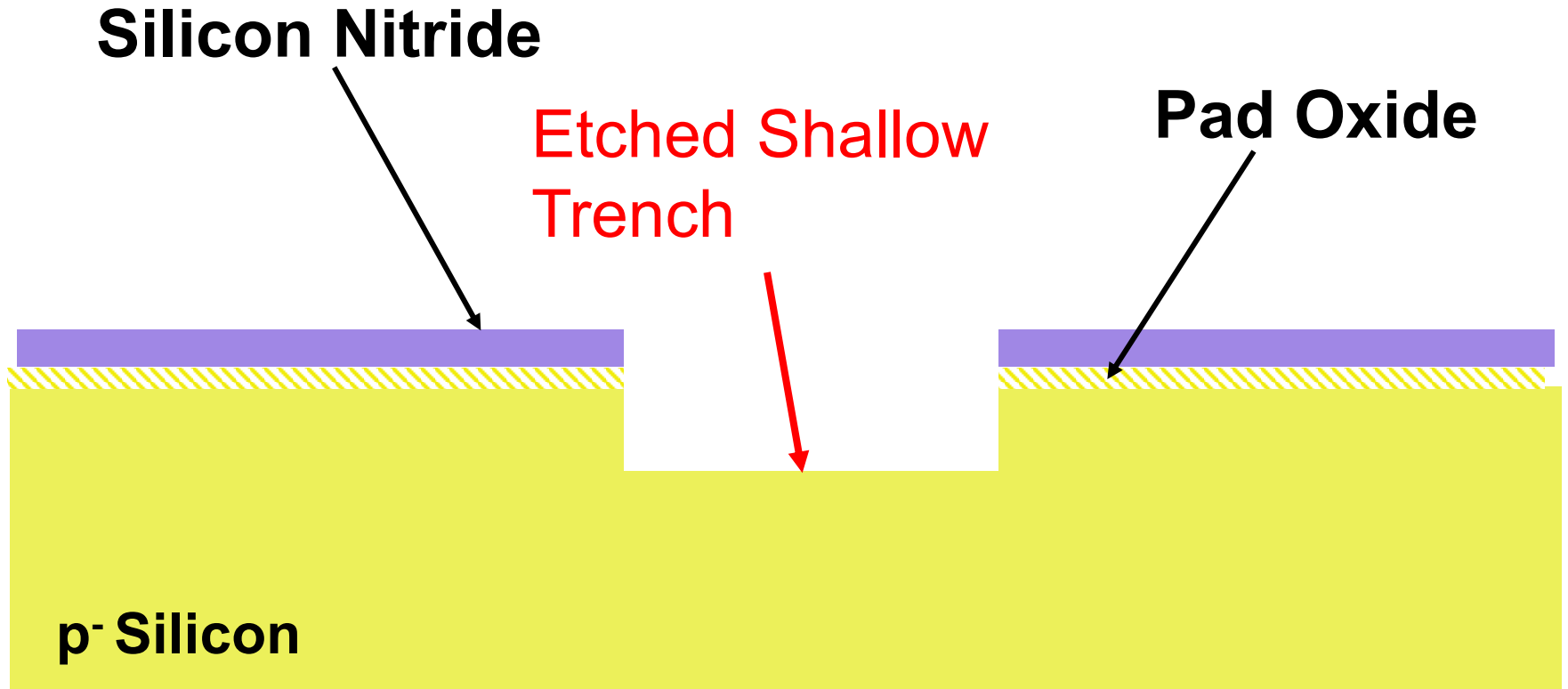
Thermally Grown SiO_2 - actual growth

Oxidation



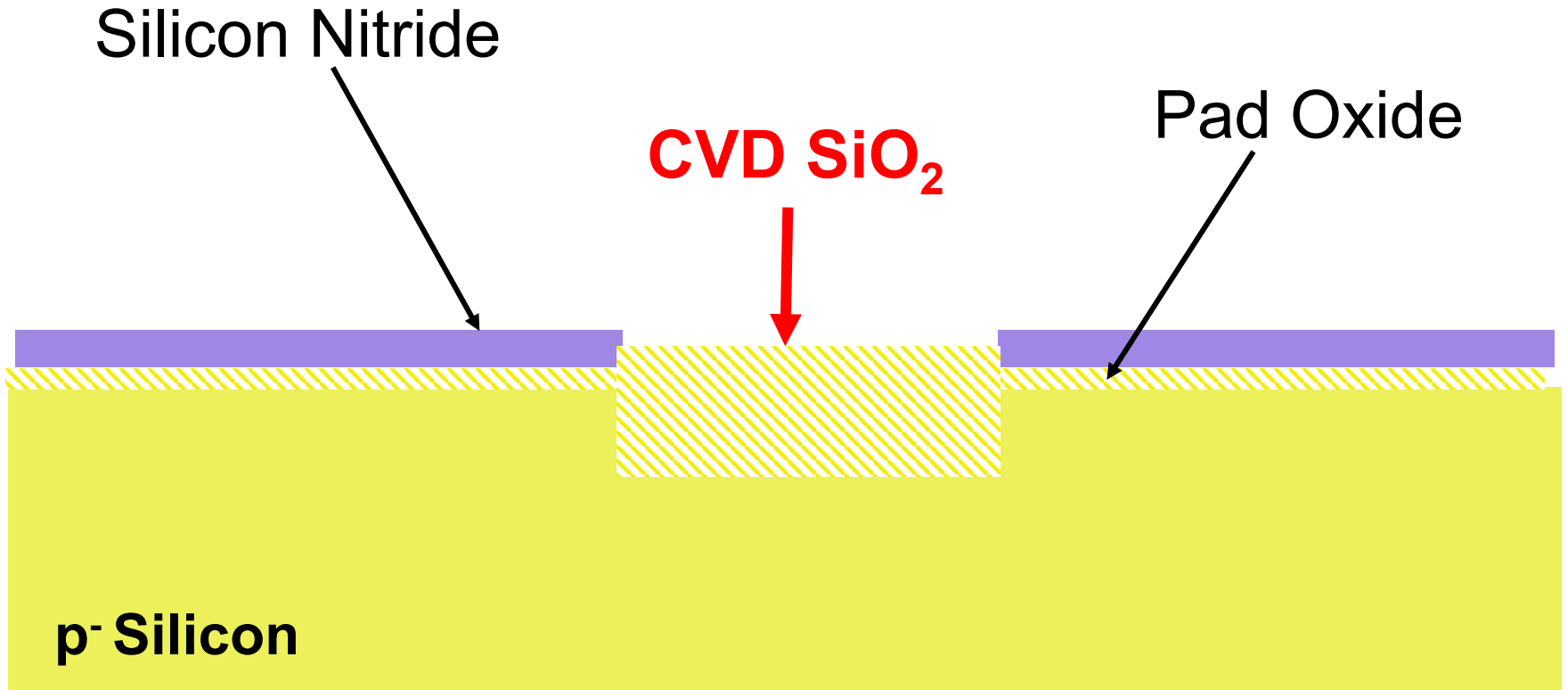
Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

Oxidation

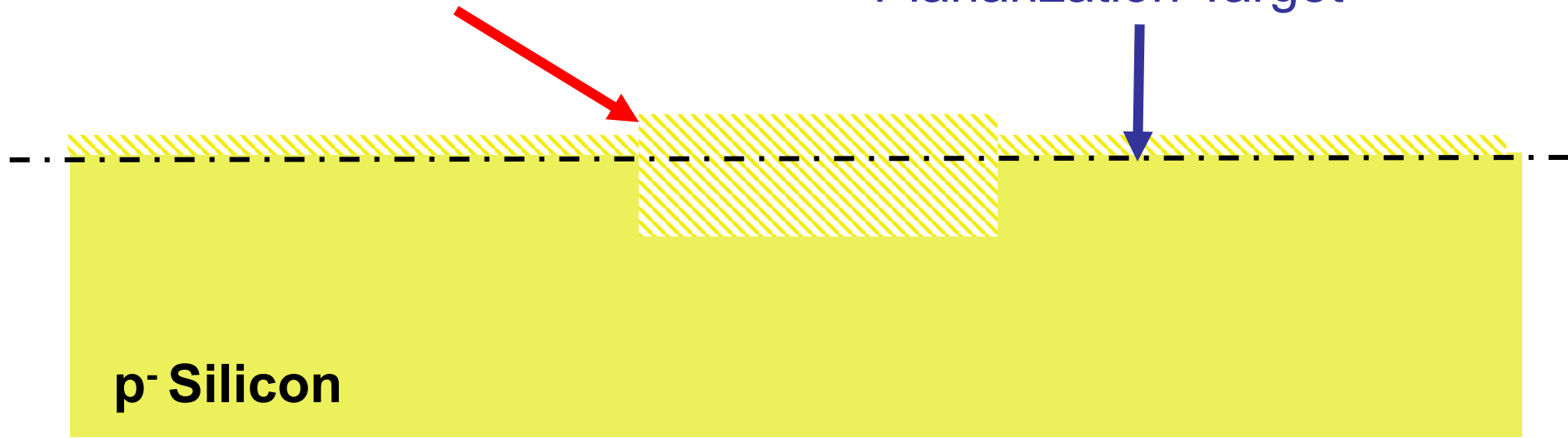


Shallow Trench Isolation (STI)

Oxidation

Planarity Improved

Planarization Target

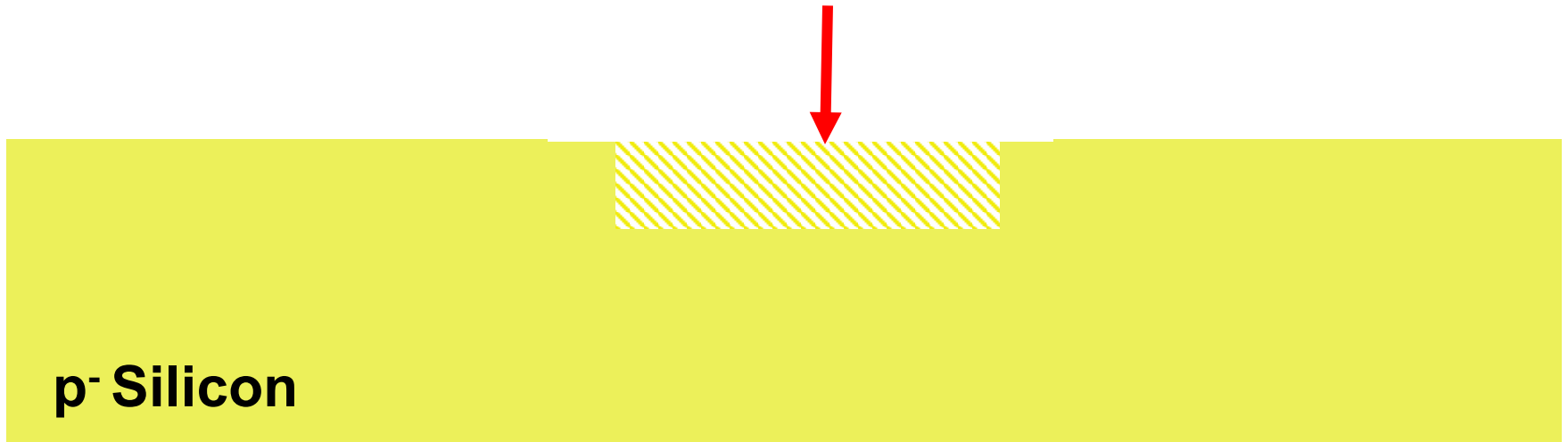


Shallow Trench Isolation (STI)

Oxidation

After Planarization

CVD SiO₂



Shallow Trench Isolation (STI)

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Epitaxy

- Single Crystalline Extension of Substrate Crystal
 - Commonly used in bipolar processes
 - CVD techniques
 - Impurities often added during growth
 - Grows slowly to allow alignment with substrate

Epitaxy

Epitaxial Layer




p-Silicon

epi can be uniformly doped or graded

Original Silicon Surface

Question: Why can't a diffusion be used to create the same effect as an epi layer ?

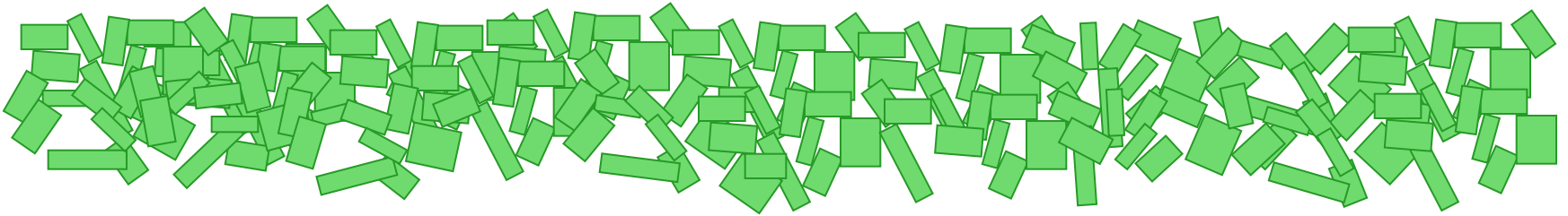
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Polysilicon

- Elemental contents identical to that of single crystalline silicon
 - Electrical properties much different
 - If doped heavily makes good conductor
 - If doped moderately makes good resistor
 - Widely used for gates of MOS devices
 - Widely used to form resistors
 - Grows fast over non-crystalline surface
 - Patterned with Photoresist/Etch process
 - Silicide often used in regions where resistance must be small
 - Refractory metal used to form silicide
 - Designer must indicate where silicide is applied (or blocked)

Polysilicon



Polysilicon



Single-Crystalline Silicon

Silicon Wafers and Solar Panels Made from Polysilicon

Where does the silicon come from?

In 2013:

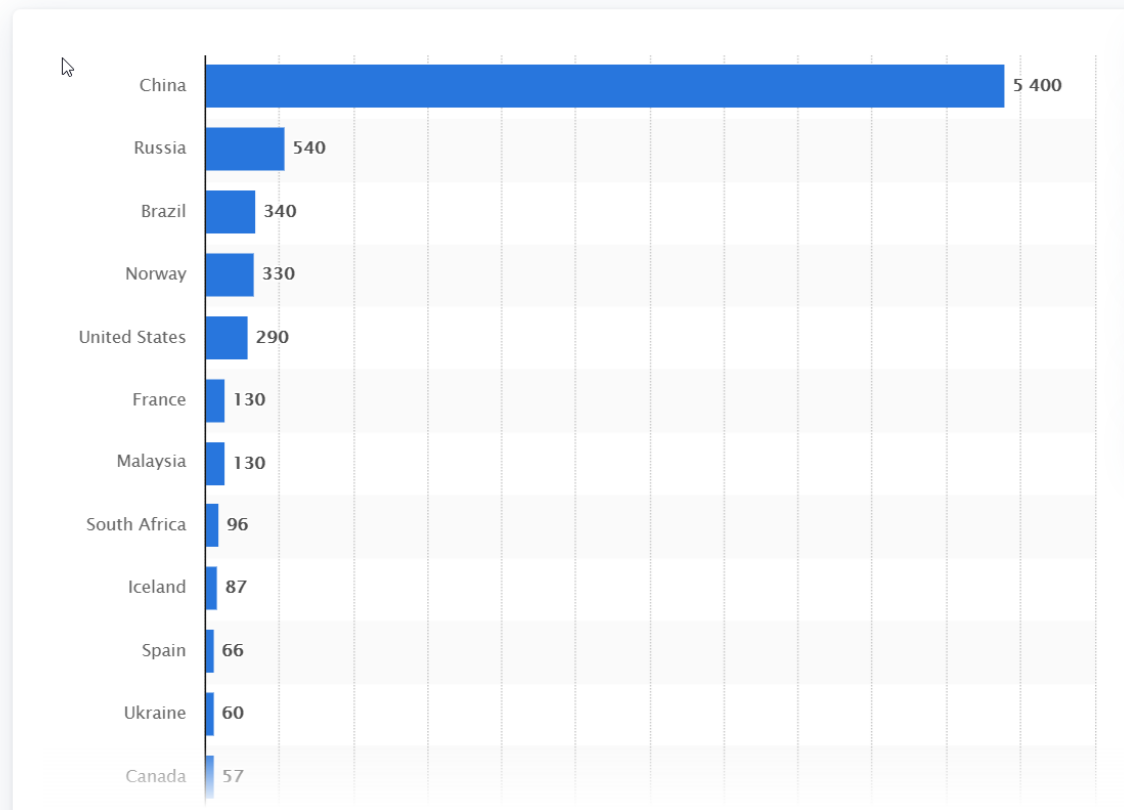
Largest polysilicon producers in 2013 (market-share in %)			
GCL-Poly Energy	China	65,000 tons	22%
Wacker Chemie	Germany	52,000 tons	17%
OCI	South Korea	42,000 tons	14%
Hemlock Semiconductor	USA	36,000 tons	12%
REC	Norway	21,500 tons	7%

Source: Market Realist cites World production capacity at 300,000 tons in 2013.^[2]
BNEF estimated actual production for 2013 at 227,000 tons^[1]

In 2020:

Major countries in silicon production worldwide in 2020

(in 1,000 metric tons)



In 2020:

The top 10 polysilicon manufacturers for 2020 include:

1. Tongwei (China)
2. Wacker (Germany/United States)
3. Daqo New Energy (China)
4. GCL-Poly (China)
5. Xinte Energy (China)
6. Xingjiang East Hope New Energy (China)
7. OCI (South Korea/Malaysia)
8. Asia Silicon (China)
9. Hemlock (United States)
10. Inner Mongolia Dongli Photovoltaic Electronics (China)

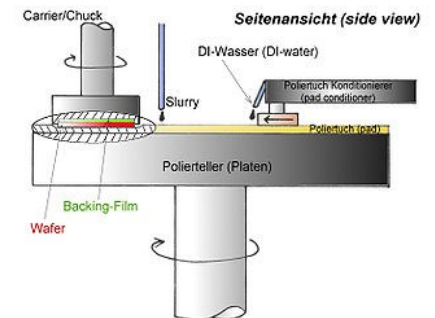
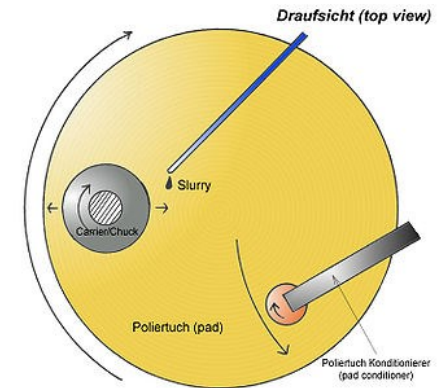
Top 4 projected to be from China by 2022

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Planarization

- Planarization used to keep surface planar during subsequent processing steps
 - Important for creating good quality layers in subsequent processing steps
 - Mechanically planarized



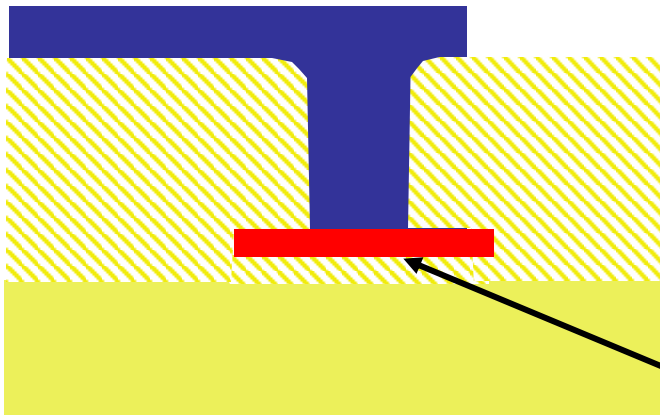
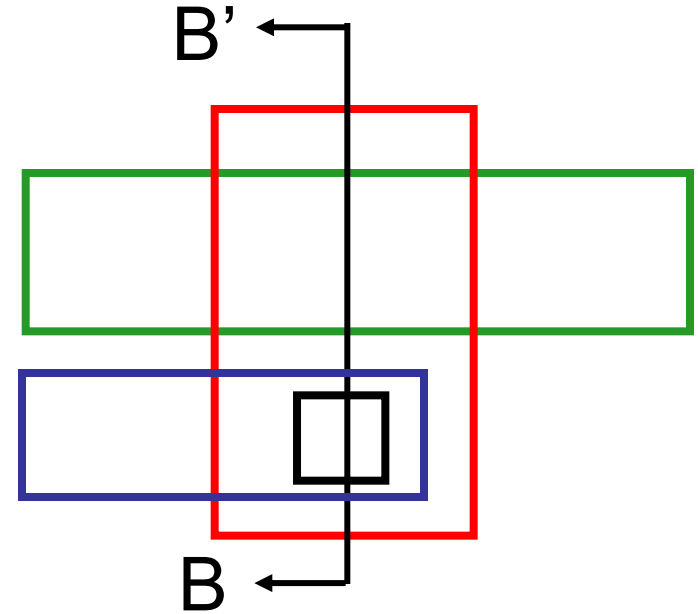
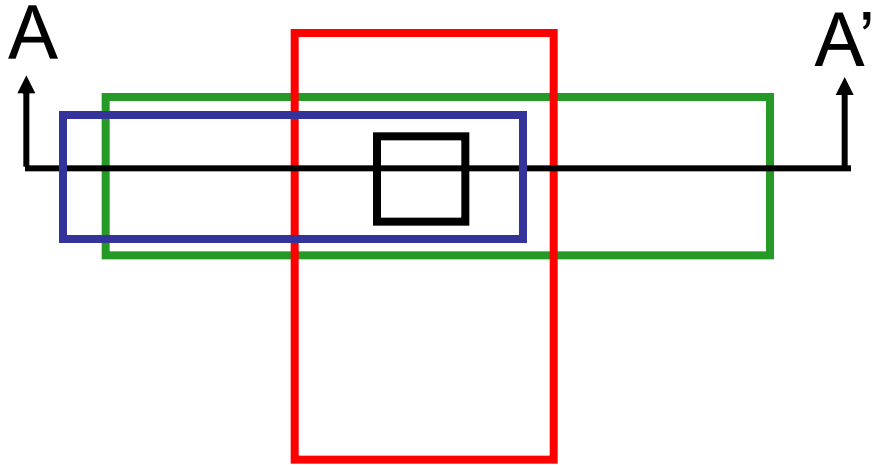
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Contacts, Interconnect and Metalization

- Contacts usually of a fixed size
 - All etches reach bottom at about the same time
 - Multiple contacts widely used
 - Contacts not allowed to Poly on thin oxide in most processes
 - Dog-bone often needed for minimum-length devices

Contacts

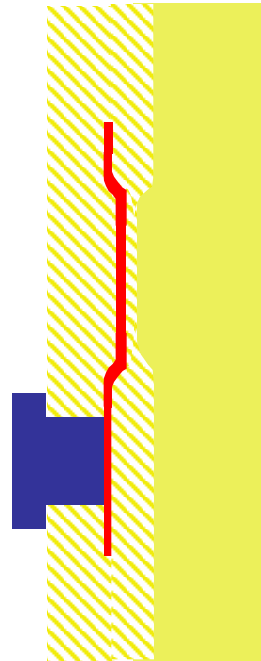
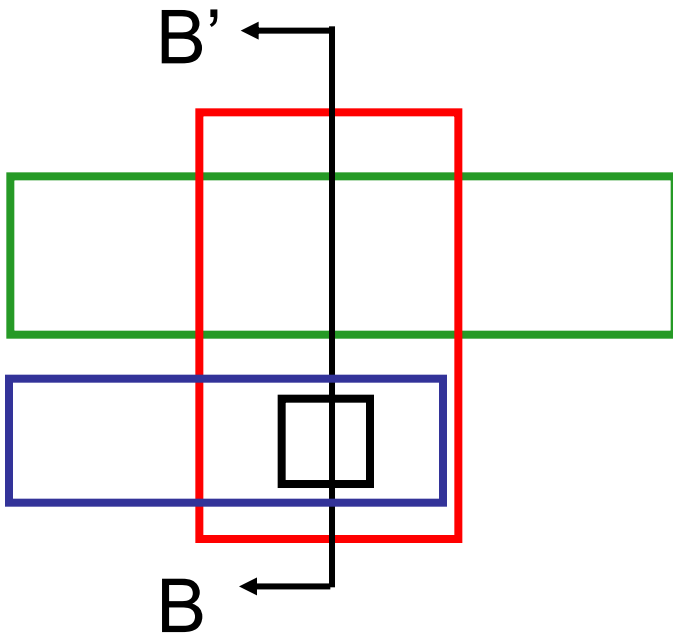


Unacceptable Contact

Acceptable Contact

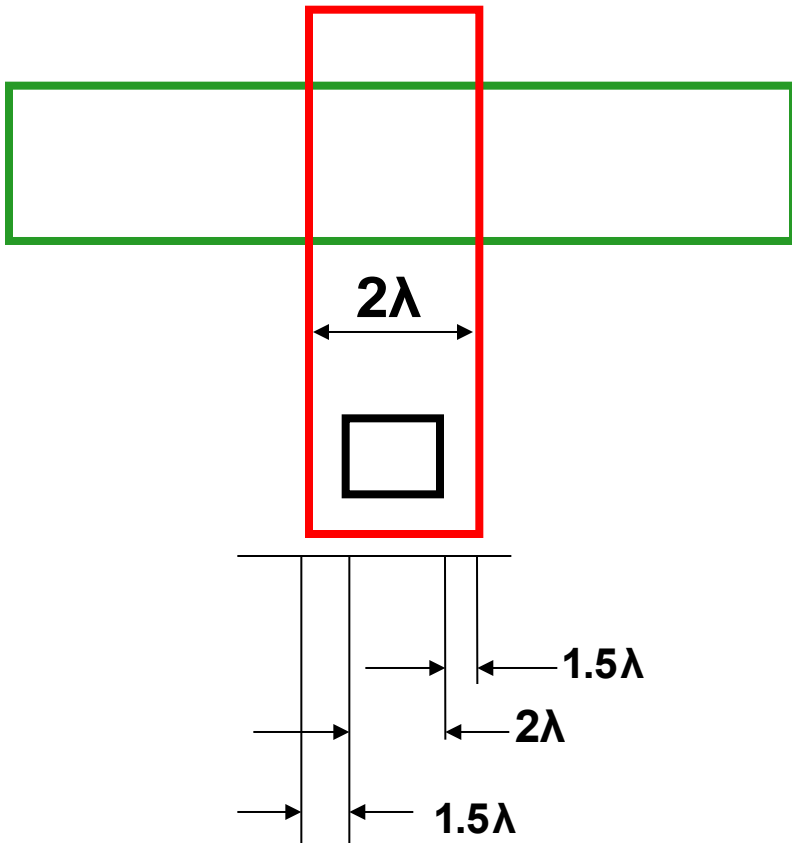
Vulnerable to pin holes
(usually all contacts are same size)

Contacts

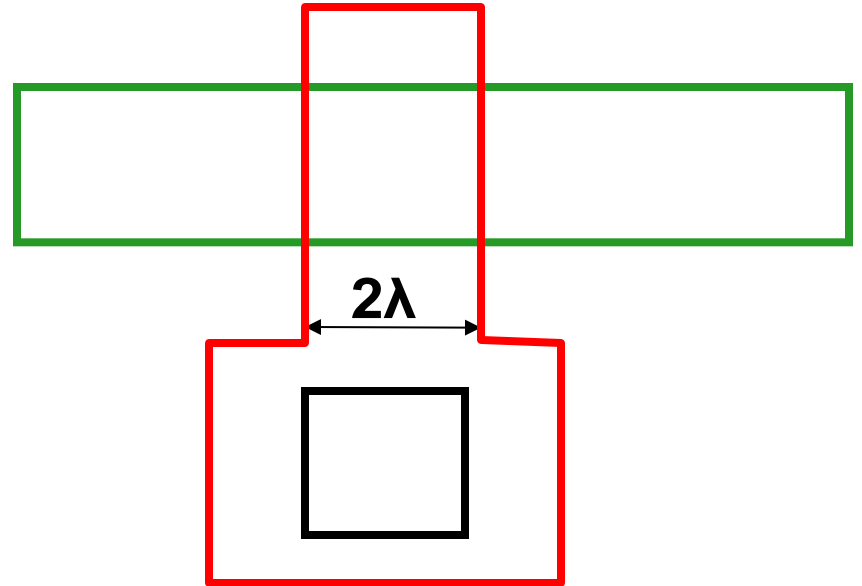


Acceptable Contact

Contacts

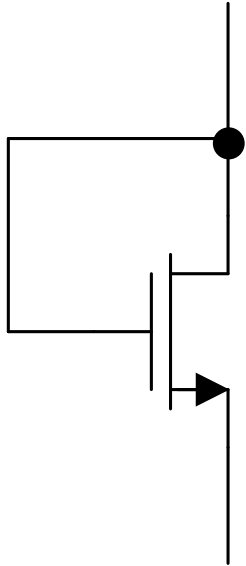


Design Rule Violation

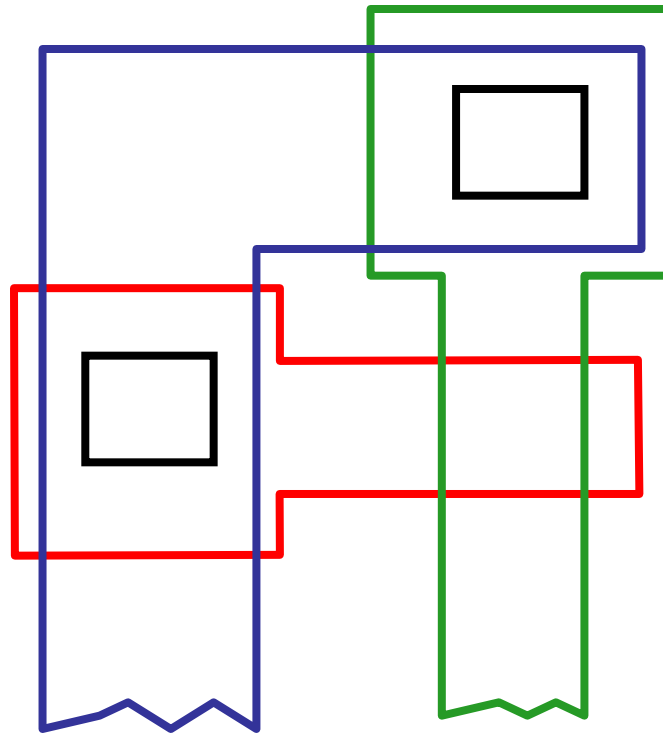


"Dog Bone" Contact

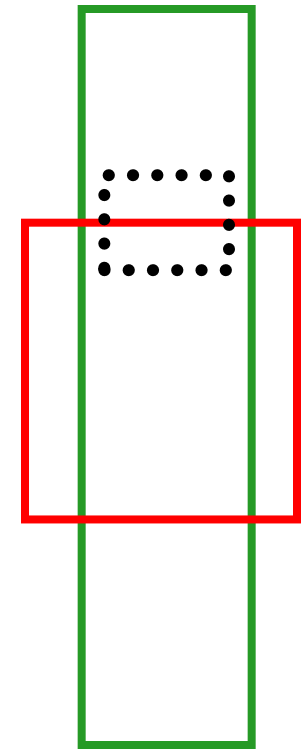
Contacts



Common
Circuit
Connection



Standard Interconnection



Buried Contact

Can save area but not
allowed in many processes



Stay Safe and Stay Healthy !

End of Lecture 10